Customer No.: 31561
Application No.: 10/707,139
Docket No.: 10243-US-PA

AMENDMENT

Please amend the application as indicated hereafter.

In the Claims :

1.-8. (canceled)

9. (original) A thin film transistor (TFT) array substrate, comprising:

a plurality of scan lines disposed on a substrate;

a plurality of first bonding pads disposed on an edge of a surface of the substrate, wherein the first bonding pads are electrically connecteded to the scan lines;

a plurality of second bonding pads disposed on another edge of the surface of the substrate;

a gate dielectric layer disposed on the substrate, wherein a portion of the first bonding pads, and the second bonding pads are exposed by the gate dielectric layer;

a plurality of data lines disposed on the gate dielectric layer, wherein the data lines are extended to the edge of the substrate and are electrically connected to the second bonding pads;

a first mask layer disposed over the gate dielectric layer partially covering the first bonding pads, wherein a remaining portion of the first bonding pads remain exposed;

a second mask layer disposed over the gate dielectric layer partially covering the second bonding pads, wherein a remaining portion of the second bonding pads remain exposed;

a plurality of thin film transistors disposed on the substrate, wherein each of the

thin film transistors comprises a gate, a source/drain, a channel layer and an ohm contact layer, each of the gates is electrically connected to each of the scan lines, each of the sources is electrically connected to each of the data lines, each of the channel layers is disposed on the gate dielectric layer over each of the gates, and each of the ohm contact layers is disposed on each of the channel layers;

a patterned cover layer covering over the thin film transistors and the gate dielectric layers;

a patterned photoresist layer disposed over the cover layer partially covering the two edges of the substrate such that the remaining portion of the two edges of the substrate are exposed; and

a plurality of pixel electrodes disposed on the photoresist layer corresponding to the disposed thin film transistors, wherein each of the pixel electrodes is electrically connected to each of the drains.

10. (original) The thin film transistor array substrate of claim 9, wherein a material of the first mask layer and the second mask layer is comprised of same as that of the source/drain and the data lines, or same as that of the channel layers and the ohm contact layers, or a combination thereof.

11. (original) The thin film transistor array substrate of claim 9, wherein the first mask layer and the second mask layer are comprised of a bilayer structure having a top layer and a bottom layer, wherein a material of the top layer is same as that of the source/drain and the data lines, and a material of the bottom layer is same as that of the channel layers and the ohm contact layers.

12. (original) The thin film transistor array substrate of claim 9, wherein the first mask layer and the second mask layer comprises a ring pattern, and covers a pherpheral region of the first bonding pads and the second bonding pads.

13. (original) The thin film transistor array substrate of claim 9, wherein the first mask layer and the second mask layer are comprised of a material same as that of the channel layers and the ohm contact layers, and the first mask layer and the second mask layer comprises a plurality of openings having rectangular patterns and cover the two edges of the substrate not covered by the photoresist layer, and wherein a portion of the first bonding pads and the second bonding pads are exposed within the openings.

14. (original) The thin film transistor array substrate of claim 9, wherein the first mask layer and the second mask layer are comprised of a material same as that of the channel layers and the ohm contact layers, and the first mask layer and the second mask layer are comprised of a single mask layer having a plurality of openings, wherein a portion of the first bonding pads and the second bonding pads are exposed within the openings.

15. (original) The thin film transistor array substrate of claim 9, wherein a plurality of first openings is formed in the photoresist layer for exposing the data lines, and a plurality of second openings is formed in the photoresist layer and the gate dielectric layer for exposing the second bonding pads, and an electrode material layer is disposed into each of the first openings and into each of the second openings for electrically connecting the data lines with the second bonding pads.

16. (original) The thin film transistor array substrate of claim 9, wherein further

comprises forming an etching stop layer over each of the channel layers over each of the gates.

17. (original) A thin film transistor (TFT) array substrate, comprising:

a plurality of scan lines disposed on a substrate;

a plurality of first bonding pads disposed over an edge of a surface of the substrate, wherein the first bonding pads are electrically connected to the scan lines;

a plurality of second bonding pads disposed over another edge of a surface of the substrate;

a gate dielectric layer disposed on the substrate, wherein a portion of the first bonding pads and the second bonding pads are exposed by the gate dielectric layer, and a thickness of the gate dielectric layer located over a peripheral region of the first bonding pads and the second bonding pads is less than a thickness of the gate dielectric layer elsewhere;

a plurality of data lines disposed on the gate dielectric layer, wherein the data lines are extended to the edge of the substrate and are electrically connected to the second bonding pads;

a plurality of thin film transistors disposed on the substrate, each of the thin film transistors comprises a gate, a source/drain, a channel layer and an ohm contact layer, each of the gates is electrically connected to each of the scan lines, each of the sources is electrically connected to each of the data lines, each of the channel layers is disposed on the gate dielectric layer over each of the gates, each of the ohm contact layers is disposed on each of the channel layers;

a patterned cover layer, covering over the thin film transistors and the gate dielectric layers;

a patterned photoresist layer, disposed over the cover layer and partially covering the two edges of the substrate such that the remaining portion over the two edges are exposed; and

a plurality of pixel electrodes, disposed on the photoresist layer corresponding to the disposed thin film transistors, wherein each of the pixel electrodes is electrically connected to each of the drains.

18. (original) The thin film transistor array substrate of claim 17, further comprises a first mask layer and a second mask layer disposed over peripheral region of the gate dielectric layers not covered by the photoresist layer covering over the first bonding pads and the second bonding pads respectively, wherein a material of the first mask layer and the second mask layer is same as that of the channel layers and the ohm contact layers.

19. (original) The thin film transistor array substrate of claim 18, wherein the first mask layer and the second mask layer comprises a ring pattern.

20. (original) The thin film transistor array substrate of claim 18, wherein the first mask layer and the second mask layer comprises a plurality of openings having rectangular patterns, wherein a portion of the first bonding pads and the second bonding pads are exposed within the openings.

21. (original) The thin film transistor array substrate of claim 18, wherein the first mask layer and the second mask layer are comprised of a single mask layer having a

plurality of openings, wherein a portion of the first bonding pads and the second bonding pads are exposed within the openings.

22. (original) The thin film transistor array substrate of claim 17, wherein a plurality of first openings is formed in the photoresist layer for exposing the data lines, and a plurality of second openings is formed in the photoresist layer and the gate dielectric layer for exposing the second bonding pads, and an electrode material layer is formed into each of the first openings and each of the second openings for electrically connecting with the data lines and the second bonding pads.

23. (original) The thin film transistor array substrate of claim 17, further comprising a step of forming an etching stop layer over the channel layers over each of the gates.